Personal Computer Hardware Reference Library

IBM 5-1/4″ Diskette Drive Adapter

6361505

Contents

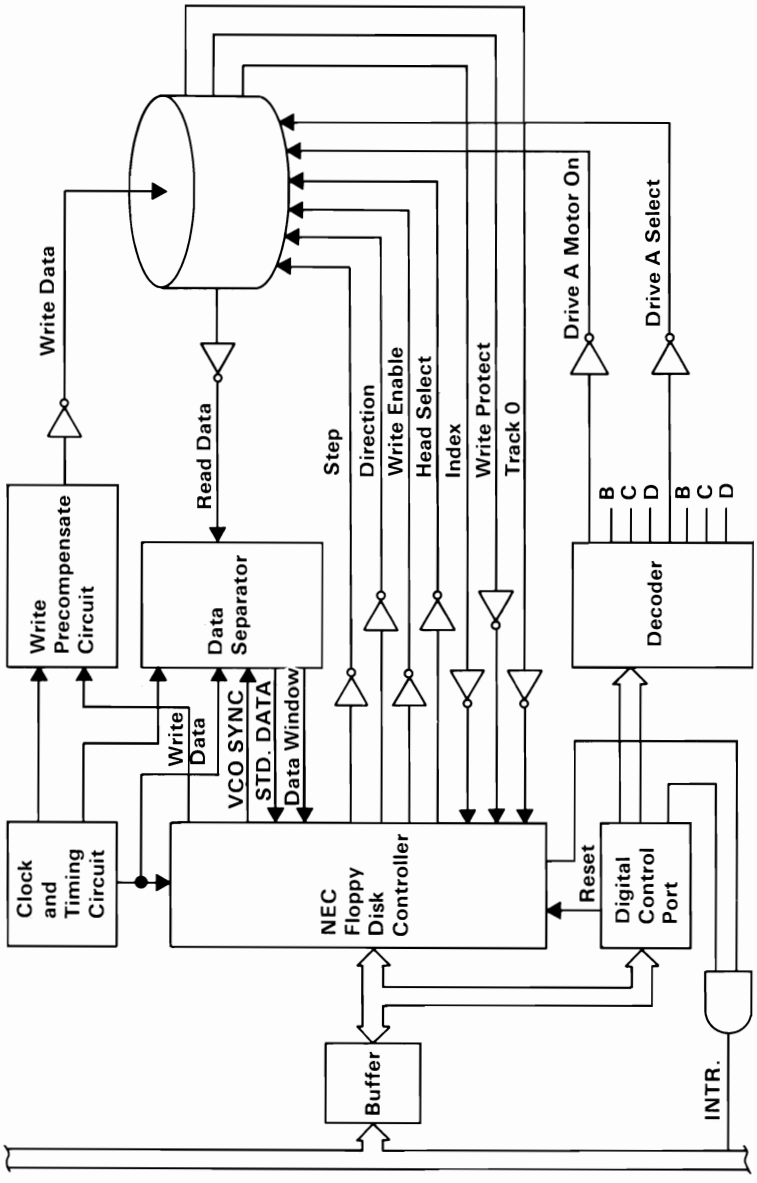
Description

The IBM 5-1/4" Diskette Drive Adapter fits into one of the expansion slots in the system unit. It is connected to one or two diskette drives through an internal, daisy-chained flat cable. The adapter has a connector at the other end that extends through the rear panel of the system unit. This connector has signals for two additional external diskette drives; thus, the 5-1/4 inch diskette drive adapter can attach four 5-1/4 inch drives — two internal and two external.

The adapter is designed for double-density, MFM-coded, diskette drives and uses write precompensation with an analog phase-lock loop for clock and data recovery. The adapter is a general-purpose device using the NEC μPD765 or equivalent controller. Therefore, the diskette drive parameters are programmable. In addition, the attachment supports the diskette drive's write-protect feature. The adapter is buffered on the I/O bus and uses the system board's direct memory access (DMA) for record data transfers. An interrupt level also is used to indicate when an operation is complete and that a status condition requires microprocessor attention.

In general, the 5-1/4 inch diskette drive adapter presents a high-level command interface to software I/O drivers.

The following is a block diagram of the IBM 5-1/4" Diskette Drive Adapter.



5-1/4 Inch Diskette Drive Adapter Block Diagram

Programming Considerations

This attachment consists of an 8-bit digital output register in parallel with a NEC μPD765 or equivalent floppy disk controller (FDC).

In the following description, drive numbers 0, 1, 2, and 3 are equivalent to drives A, B, C, and D.

Digital-Output Register

The Digital-Output register (DOR) is an output-only register used to control drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface 'reset' line. The bits have the following functions:

Bits 0 and 1 These bits are decoded by the hardware to select one drive if its motor is on:

Bit 1 0	Drive
0 0	0 (A)
0 1	1 (B)
1 0	2 (C)
1 1	3 (D)

Bit 2 The FDC is held reset when this bit is clear. It must be set by the program to enable the FDC.

Bit 3 This bit allows the FDC interrupt and DMA requests to be gated onto the I/O interface. If this bit is cleared, the interrupt and DMA request I/O interface drivers are disabled.

Bits 4, 5, 6, and 7 These bits control, respectively, the motors of drives 0, 1, 2 (A, B, C), and 3 (D). If a bit is clear, the associated motor is off, and the drive cannot be selected.

Floppy Disk Controller

The floppy disk controller (FDC) contains two registers that may be accessed by the system unit's microprocessor: a status register and a data register. The 8-bit main status register contains the status information of the FDC and may be accessed at any time. The 8-bit data register (actually consisting of several registers in a stack with only one register presented to the data bus at a time) stores data, commands, parameters, and provides floppy disk drive (FDD) status information. Data bytes are read from or written to the data register in order to program or obtain results after a particular command. The main status register can only be read and is used to facilitate the transfer of data between the system unit's microprocessor and FDC.

The bits in the main status register (hex 34F) are defined as follows:

Bit Number	Name	Symbol	Description
DB0	FDD A Busy	DAB	FDD number 0 is in the Seek mode.
DB1	FDD B Busy	DBB	FDD number 1 is in the Seek mode.
DB2	FDD C Busy	DCB	FDD number 2 is in the Seek mode.
DB3	FDD D Busy	DDB	FDD number 3 is in the Seek mode.
DB4	FDC Busy	CB	A read or write command is in process.
DB5	Non-DMA Mode	NDM	The FDC is in the non-DMA mode.
DB6	Data Input/ Output	DIO	Indicates direction of data transfer between FDC and processor. If DIO = "1," then transfer is from FDC data register to the processor. If DIO = "0," then transfer is from the processor to FDC data register.
DB7	Request for Master	RQM	Indicates data register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

The FDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the system unit's microprocessor, and the result after execution of the command may also be a multi-byte transfer back to the system

unit's microprocessor. Because of this multi-byte interchange of information between the FDC and the system unit's microprocessor, it is convenient to consider each command as consisting of three phases:

Command Phase

The FDC receives all information required to perform a particular operation from the system unit's microprocessor.

Execution Phase

The FDC performs the operation it was instructed to do.

Result Phase

After completion of the operation, status and other housekeeping information are made available to the system unit's microprocessor.

The following tables define the symbols used in the command summary. The command summary immediately follows these tables.

Symbol	Name	Description
A0	Address Line 0	A0 controls selection of main status register (A0 = 0) or data register (A0 = 1).
C	Cylinder Number	C stands for the current/selected cylinder (track) number of the medium.
D	Data	D stands for the data pattern that is going to be written into a sector.
D7-D0	Data Bus	8-bit data bus, where D7 stands for a most significant bit, and D0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length that users are going to read from or write to the sector.
EOT	End of Track	EOT stands for the final sector number on a cylinder.
GPL	Gap Length	GPL stands for the length of gap 3 (spacing between sectors excluding VCO sync field).
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1. (H = HD in all command words).
HLT	Head Load Time	HLT stands for the head load time in the FDD (4 to 512 ms in 4-ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (0 to 480 ms in 32-ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected; if it is high, MFM mode is selected only if MFM is implemented.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. (A cylinder under both HD0 and HD1 will be read or written.)
N	Number	N stands for the number of data bytes written in a sector.

Symbol Descriptions (Part 1 of 2)

Symbol	Name	Description
NCN	New Cylinder Number	NCN stands for a new cylinder number which is going to be reached as a result of the seek operation. (Desired position of the head.)
ND	Non-DMA Mode	ND stands for operation in the non-DMA mode.
PCN	Present Cylinder Number	PCN stands for cylinder number at the completion of sense-interrupt-status command indicating the position of the head at present time.
R	Record	R stands for the sector number, which will be read or written.
R/W	Read/Write	R/W stands for either read (R) or write (W) signal.
SC	Sector	SC indicates the number of sectors per cylinder.
SK	Skip	SK stands for skip deleted-data address mark.
SRT	Step Rate Time	SRT stands for the stepping rate for the FDD (2 to 32 ms in 2-ms increments).
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST0-3 stand for one of four registers that store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A0 = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP	Scan Test	During a scan operation, if STP = 1, the data in contiguous sectors is compared byte-by-byte with data sent from the processor (or DMA), and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number encoded the same as bits 0 and 1 of the digital output register (DOR).

Symbol Descriptions (Part 2 of 2)

Command Summary

In the following table, 0 indicates "logical 0" for that bit, 1 means "logical 1," and X means "don't care."

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		Read Data								
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W				C					Sector ID information
	W				H					prior to command
	W				R					execution.
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and main system.
Result	R				ST 0					Status information
	R				ST 1					after command
	R				ST 2					execution.
	R				C					Sector ID information
	R				H					after command
	R				R					execution.
	R				N					
		Read Deleted Data								
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W				C					Sector ID information
	W				H					prior to command
	W				R					execution.
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and main system.
Result	R				ST 0					Status information
	R				ST 1					after command
	R				ST 2					execution.
	R				C					Sector ID information
	R				H					after command
	R				R					execution.
	R				N					

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		Write Data								
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W				C					Sector ID information
	W				H					prior to command
	W				R					execution.
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the main system and FDD.
Result	R				ST 0					Status information
	R				ST 1					after command
	R				ST 2					execution.
	R				C					Sector ID information
	R				H					after command
	R				R					execution.
	R				N					
		Write Deleted Data								
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W				C					Sector ID information
	W				H					prior to command
	W				R					execution.
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and main system.
Result	R				ST 0					Status ID information
	R				ST 1					after command
	R				ST 2					execution.
	R				C					Sector ID information
	R				H					after command
	R				R					execution.
	R				N					

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		Read a Track								
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W				C					Sector ID information
	W				H					prior to command
	W				R					execution.
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and main system. FDC reads all of cylinder's contents from index hole to EOT.
Result	R				ST 0					Status information
	R				ST 1					after command
	R				ST 2					execution.
	R				C					Sector ID information
	R				H					after command
	R				R					execution.
	R				N					
		Read ID								
Command	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the cylinder is stored in data register.
Result	R				ST 0					Status information
	R				ST 1					after command
	R				ST 2					execution.
	R				C					Sector ID information
	R				H					during execution
	R				R					phase.
	R				N					

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		Format a Track								
Command	W	0	MF	0	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sector/Track
	W	GPL								Gap 3
	W	D								filler byte.
Execution										FDC formats an entire cylinder.
Result	R	ST 0								Status information
	R	ST 1								after command
	R	ST 2								execution.
	R	C								In this case, the ID
	R	H								information has no
	R	R								meaning.
	R	N								
		Scan Equal								
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information
	W	H								prior to command
	W	R								execution.
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and the main system.
Result	R	ST 0								Status information
	R	ST 1								after Command
	R	ST 2								execution.
	R	C								Sector ID information
	R	H								after command
	R	R								execution.
	R	N								

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		Scan Low or Equal								
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information
	W	H								prior to command
	W	R								execution.
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST 0								Status information
	R	ST 1								after command
	R	ST 2								execution.
	R	C								Sector ID information
	R	H								after command
	R	R								execution.
	R	N								
		Scan High or Equal								
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information
	W	H								prior to command
	W	R								execution.
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST 0								Status information
	R	ST 1								after command
	R	ST 2								execution.
	R	C								Sector ID information
	R	H								after command
	R	R								execution.
	R	N								

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		Recalibrate								
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution No Result Phase										Head retracted to track 0
		Sense Interrupt Status								
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R				ST 0					Status information at the end of seek operation about the FDC
	R				PCN					
		Specify								
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	—SRT—						HUT—		
	W	—HLT—							ND	
No Result Phase										
		Sense Drive Status								
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	R				ST 3					Status information about FDD.
		Seek								
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W				NCN					
Execution										Head is positioned over proper cylinder on diskette.
No Result Phase										
		Invalid								
Command	W	Invalid Codes								Invalid command codes (NoOp — FDC goes into standby state).
Result	R				ST 0					ST 0 = 80.

Bit			Description
No.	Name	Symbol	
D7 D6	Interrupt Code	IC	D7 = 0 and D6 = 0 Normal termination of command (NT). Command was completed and properly executed. D7 = 0 and D6 = 1 Abnormal termination of command (AT). Execution of command was started, but was not successfully completed. D7 = 1 and D6 = 0 Invalid command issue (IC). Command that was issued was never started. D7 = 1 and D6 = 1 Abnormal termination because, during command execution, the ready signal from FDD changed state.
D5	Seek End	SE	When the FDC completes the seek command, this flag is set to 1 (high).
D4	Equipment Check	EC	If a fault signal is received from the FDD, or if the track 0 signal fails to occur after 77 step pulses (recalibrate command), then this flag is set.
D3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to side 1 of a single-sided drive, then this flag is set.
D2	Head Address	HD	This flag is used to indicate the state of the head at interrupt.
D1 D0	Unit Select 1 Unit Select 0	US 1 US 0	These flags are used to indicate a drive unit number at interrupt.

Command Status Register 0

Bit			Description
No.	Name	Symbol	
D7	End of Cylinder	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D6	—	—	Not used. This bit is always 0 (low).
D5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D4	Over Run	OR	If the FDC is not serviced by the main system during data transfers within a certain time interval, this flag is set.
D3	—	—	Not used. This bit is always 0 (low).
D2	No Data	ND	During execution of a read data, write deleted data, or scan command, if the FDC cannot find the sector specified in the ID register, this flag is set. During execution of the read ID command, if the FDC cannot read the ID field without an error, then this flag is set. During the execution of the read a cylinder command, if the starting sector cannot be found, then this flag is set.
D1	Not Writable	NW	During execution of a write data, write deleted data, or format-a-cylinder command, if the FDC detects a write-protect signal from the FDD, then this flag is set.
D0	Missing Address Mark	MA	If the FDC cannot detect the ID address mark, this flag is set. Also, at the same time, the MD (missing address mark in the data field) of status register 2 is set.

Command Status Register 1

Bit			Description
No.	Name	Symbol	
D7	—	—	Not used. This bit is always 0 (low).
D6	Control Mark	CM	During execution of the read data or scan command, if the FDC encounters a sector that contains a deleted data address mark, this flag is set.
D5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data, then this flag is set.
D4	Wrong Cylinder	WC	This bit is related to the ND bit, and when the contents of C on the medium are different from that stored in the ID register, this flag is set.
D3	Scan Equal Hit	SH	During execution of the scan command, if the condition of "equal" is satisfied, this flag is set.
D2	Scan Not Satisfied	SN	During execution of the scan command, if the FDC cannot find a sector on the cylinder that meets the condition, then this flag is set.
D1	Bad Cylinder	BC	This bit is related to the ND bit, and when the contents of C on the medium are different from that stored in the ID register, and the contents of C is FF, then this flag is set.
D0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a data address mark or deleted data address mark, then this flag is set.

Command Status Register 2

Bit			Description
No.	Name	Symbol	
D7	Fault	FT	This bit is the status of the fault signal from the FDD.
D6	Write Protected	WP	This bit is the status of the write-protected signal from the FDD.
D5	Ready	RY	This bit is the status of the ready signal from the FDD.
D4	Track 0	T0	This bit is the status of the track 0 signal from the FDD.
D3	Two Side	TS	This bit is the status of the two-side signal from the FDD.
D2	Head Address	HD	This bit is the status of the side-select signal from the FDD.
D1	Unit Select 1	US 1	This bit is the status of the unit-select-1 signal from the FDD.
D0	Unit Select 0	US 0	This bit is the status of the unit-select-0 signal from the FDD.

Command Status Register 3

Programming Summary

FDC Data Register I/O Address Hex 3F5

FDC Main Status Register I/O Address Hex 3F4

Digital Output Register I/O Address Hex 3F2

Bit 0	Drive	00: DR #A 10: DR #C
1	Select	01: DR #B 11: DR #D
2	Not FDC Reset	
3	Enable INT & DMA Requests	
4	Drive A Motor Enable	
5	Drive B Motor Enable	
6	Drive C Motor Enable	
7	Drive D Motor Enable	

All bits cleared with channel reset.

DPC Registers

FDC Constants (in hex)

N:	02	GPL Format:	05
SC:	08	GPL R/W:	2A
HUT:	F	HLT:	01
SRT:	C	(6 ms track-to-track)	

Drive Constants

Head Load	35 ms
Head Settle	15 ms
Motor Start	250 ms

Comments

- Head loads with drive select, wait HD load time before R/W.
- Following access, wait HD settle time before R/W.
- Drive motors should be off when not in use. Only A or B and C or D may run simultaneously. Wait motor start time before R/W.
- Motor must be on for drive to be selected.
- Data errors can occur while using a home television as the system display. Placing the TV too close to the diskette area can cause this to occur. To correct the problem, move the TV away from, or to the opposite side of the system unit.

System I/O Channel Interface

All signals are TTL-compatible:

Most Positive Up Level	+ 5.5 Vdc
Least Positive Up Level	+ 2.7 Vdc
Most Positive Down Level	+ 0.5 Vdc
Least Positive Down Level	− 0.5 Vdc

The following lines are used by this adapter.

+D0–7 (Bidirectional, Load: 1 74LS, Driver: 74LS 3-state): These eight lines form a bus through which all commands, status, and data are transferred. Bit 0 is the low-order bit.

+A0–9 (Adapter input, Load: 1 74LS): These 10 lines form an address bus by which a register is selected to receive or supply the byte transferred through lines D0–7. Bit 0 is the low-order bit.

+AEN (Adapter input, load: 1 74LS): The content of lines A0–9 is ignored if this line is active.

-IOW (Adapter input, Load: 1 74LS): The content of lines D0–7 is stored in the register addressed by lines A0–9 or DACK2 at the trailing edge of this signal.

-IOR (Adapter input, Load: 1 74LS): The content of the register addressed by lines A0–9 or DACK2 is gated onto lines D0–7 when this line is active.

-DACK2 (Adapter input, load: 2 74LS): This line being active degates output DRQ2, selects the FDC data register as the source or destination of bus D0–7, and indirectly gates T/C to IRQ6.

+T/C (Adapter input, load: 4 74LS): This line along with DACK2 being active indicates that the byte of data for which the DMA count was initialized is now being transferred.

+RESET (Adapter input, load: 1 74LS): An up level ends any operation in process and clears the digital output register (DOR).

+DRQ2 (Adapter output, driver: 74LS 3-state): This line is made active when the attachment is ready to transfer a byte of data to or from main storage. The line is made inactive by DACK2 becoming active or an I/O read of the FDC data register.

+IRQ6 (Adapter output, driver: 74LS 3-state): This line is made active when the FDC has completed an operation. It results in an interrupt to a routine that should examine the FDC result bytes to reset the line and determine the ending condition.

Drive A and B Interface

All signals are TTL-compatible:

Most Positive Up Level	+ 5.5 Vdc
Least Positive Up Level	+ 2.4 Vdc
Most Positive Down Level	+ 0.4 Vdc
Least Positive Down Level	– 0.5 Vdc

All adapter outputs are driven by open-collector gates. The drives must provide termination networks to Vcc (except 'motor enable', which has a 2,000-ohm resistor to Vcc).

Each adapter input is terminated with a 150-ohm resistor to Vcc.

Adapter Outputs

-Drive Select A and B

(Driver: 7438): These two lines are used by drives A and B to degate all drivers to the adapter and receivers from the attachment (except 'motor enable') when the line associated with a drive is inactive.

-Motor Enable A and B

(Driver: 7438): The drive associated with each of these lines must control its spindle motor such that it starts when the line becomes active and stops when the line becomes inactive.

-Step

(Driver: 7438): The selected drive moves the read/write head one cylinder in or out per the direction line for each pulse present on this line.

-Direction

(Driver: 7438): For each recognized pulse of the 'step' line, the read/write head moves one cylinder toward the spindle if this line is active, and away from the spindle if inactive.

-Head Select

(Driver: 7438): Head 1 (upper head) will be selected when this line is active (low).

-Write Data

(Driver: 7438): For each inactive-to-active transition of this line while 'write enable' is active, the selected drive causes a flux change to be stored on the diskette.

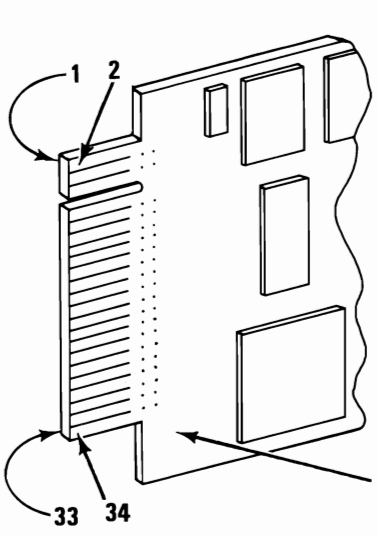
-Write Enable

(Driver: 7348): The drive disables write current in the head unless this line is active.

Adapter Inputs

-Index	The selected drive must supply one pulse per diskette revolution on this line.
-Write Protect	The selected drive must make this line active if a write-protected diskette is in the drive.
-Track 0	The selected drive must make this line active if the read/write head is over track 0.
-Read Data	The selected drive supplies a pulse on this line for each flux change encountered on the diskette.

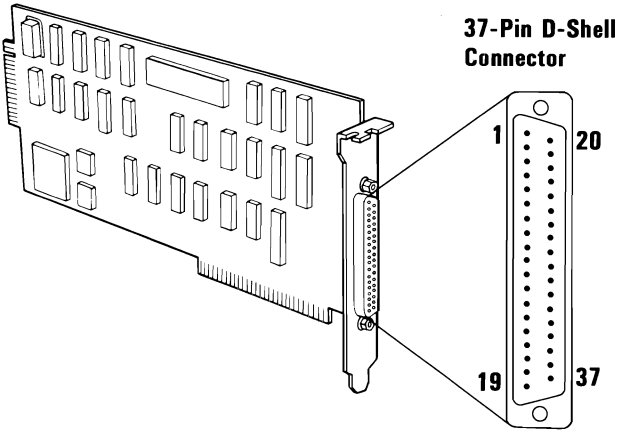
Specifications



Note: Lands 1-33 (odd numbers) are on the back of the board. Lands 2-34 (even numbers) are on the front, or component side.

	At Standard TTL Levels	Land Number	
	Ground-Odd Numbers	1-33	
	Unused	2,4,6	
	Index	8	→
	Motor Enable A	10	←
	Drive Select B	12	←
	Drive Select A	14	←
	Motor Enable B	16	←
Diskette Drives	Direction (Stepper Motor)	18	← Drive Adapter
	Step Pulse	20	←
	Write Data	22	←
	Write Enable	24	←
	Track 0	26	→
	Write Protect	28	→
	Read Data	30	→
	Select Head 1	32	←
	Unused	34	

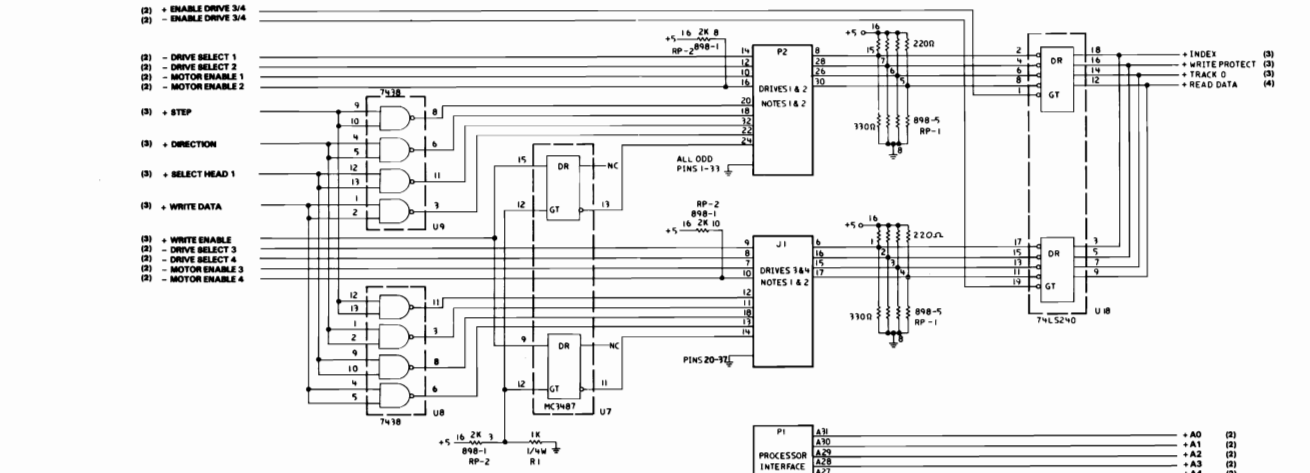
Connector Specifications (Part 1 of 2)



	At Standard TTL Levels	Pin Number	
	Unused	1-5	
	Index	6	→
←	Motor Enable C	7	
←	Drive Select D	8	
←	Drive Select C	9	
←	Motor Enable D	10	
←	Direction (Stepper Motor)	11	
←	Step Pulse	12	
←	Write Data	13	
←	Write Enable	14	
←	Track 0	15	→
	Write Protect	16	→
	Read Data	17	→
←	Select Head 1	18	
	Ground	20-37	

External Drives — Drive Adapter

Connector Specifications (Part 2 of 2)



NOTES:

1 SIGNALS ON DRIVE PINS 10 THRU 16 ARE SWAPPED BY THE DRIVE CABLE BETWEEN DRIVES 1 & 2 (AND 3 & 4) AS FOLLOWS:

10	16
11	15
12	14
13	13
14	12
15	11
16	10

2 ALL DRIVES ARE JUMPERED FOR MULTIPLEX OPERATION. HEAD LOAD WITH DRIVE SELECT AND DRIVE SELECT VIA INPUT PIN 12. TERMINATING R-PACS ARE LEFT IN DRIVES 1 & 3 ONLY

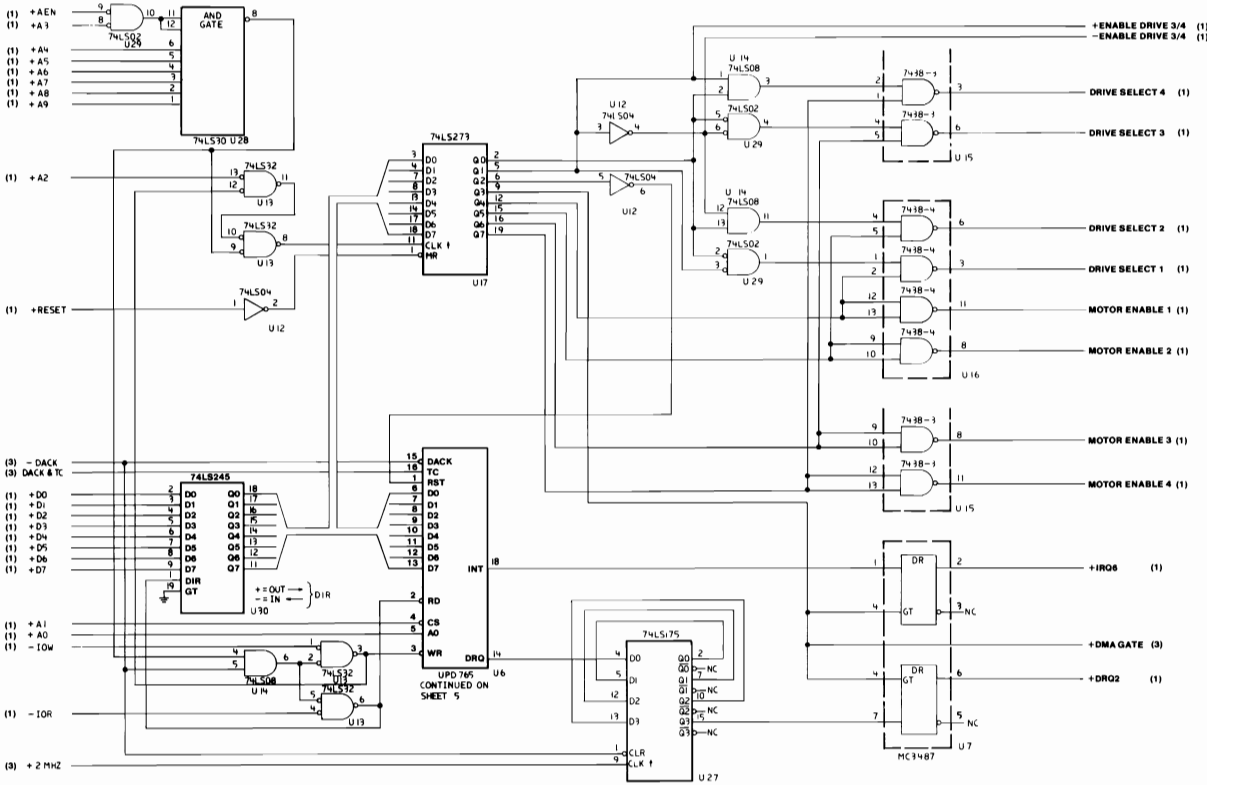
3 .047 μFD SHOULD BE ADJACENT TO MODULES MC3487, 7438, 74S74, 16 MHZ OSC, RP-1, MCM4049, MC4024, 74LS161 & 74LS191 8.2 μFD CAPS SHOULD BE NEAR ASSOCIATED M PINS

4 ALL SIGNAL LINES HIGHER THAN OR EQUAL TO 1 MHZ SHOULD BE KEPT TO THE SHORTEST POSSIBLE LENGTH. THIS IS A PRIMARY DESIGN GOAL

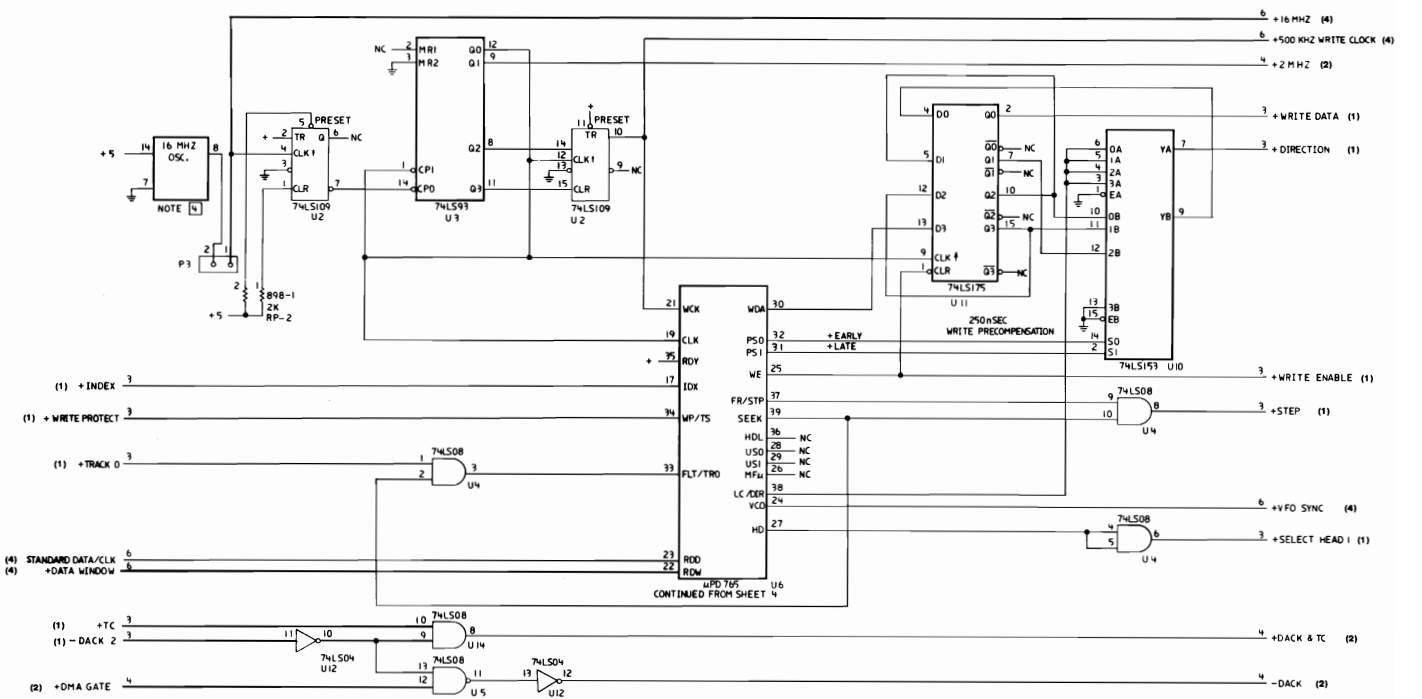
5 MAKE NO CONNECTION TO UNUSED PINS ON THE VCO, CHARGE PUMP & DATA SEPARATOR MODULES

6 ALL VOLTAGE AND GROUND CONNECTIONS TO THE VCO, CHARGE PUMP AND ASSOCIATED DISCRETE COMPONENTS SHOULD BE SEPARATE FROM OTHER CIRCUITS AND THEN JOINED TO THE OTHER CIRCUITS AT ONE POINT

5-1/4 Inch Diskette Drive Adapter (Sheet 1 of 4)

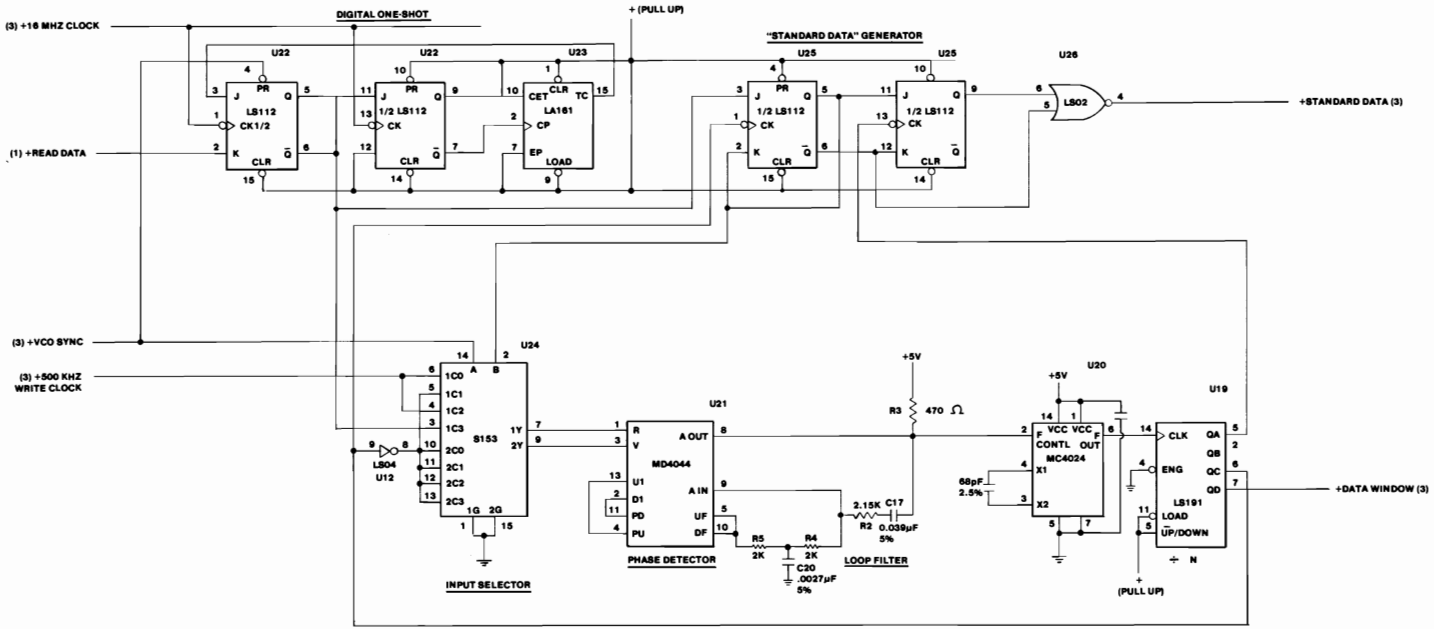


5-1/4 Inch Diskette Drive Adapter (Sheet 2 of 4)



NOTE: U4 (74LS08) PINS 12 AND 13 ARE CONNECTED ONLY ON CARDS BUILT USING RAW CARD P/N 5001293

5-1/4 Inch Diskette Drive Adapter (Sheet 3 of 4)



5-1/4 Inch Diskette Drive Adapter (Sheet 4 of 4)