μPD27C256A
32,768 x 8-BIT
CMOS UV/OTP EPROM

Description

The μPD27C256A is a 262,144-bit ultraviolet erasable and electrically programmable read-only memory utilizing CMOS double-polysilicon technology. The device is organized as 32K words by 8 bits and operates from a single +5 V power supply. All inputs and outputs are TTL-compatible. The μPD27C256A has single location programming, three-state outputs and is pin-compatible with the 27256 EPROM. It is available as a 28-pin DIP.

The μPD27C256A is available in a cerdip package with a quartz window as an ultraviolet (UV) erasable EPROM, or in a plastic package as a one-time-programmable (OTP) non-erasable EPROM. High density surface mount packages are available for both UV and OTP versions.

The μPD27C256A has a program voltage (V_{PP}) of 12.5 V.

Features

- ☐ 32K-word by 8-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ Single location programming
- ☐ High-speed programming mode
- ☐ Low power dissipation,
  - —Active: 165 mW
  - —Standby: 550 μW
- ☐ Input/output TTL-compatible for reading and programming
- ☐ Single +5 V ± 10% power supply
- ☐ JEDEC vendor identification mode
- ☐ Three-state outputs
- ☐ Pin-compatible with μPD27256 EPROM
- ☐ CMOS double-polysilicon technology
- ☐ 28-pin DIP, plastic miniflat, or 32-pin ceramic LCC packages

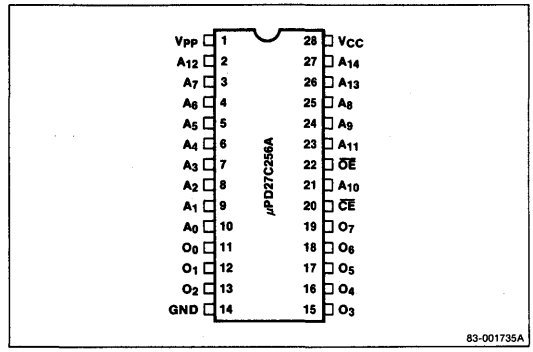
Performance Ranges

Device	Access Time (Max)	Power Supply (Max) Active	Standby
μPD27C256A-12	120 ns	30 mA	100 μA
μPD27C256A-15(1)	150 ns	30 mA	100 μA
μPD27C256A-20(1)	200 ns	30 mA	100 μA

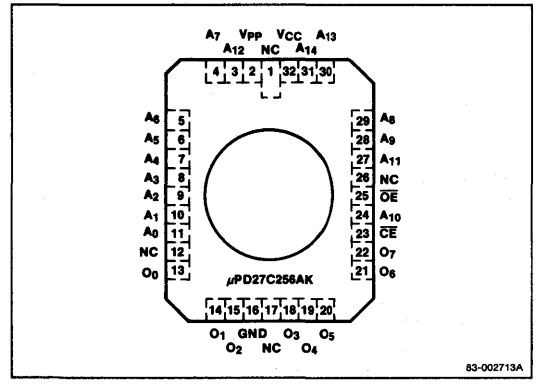
Note:
(1) Available as either UV or OTP. OTP version is *preliminary*.

Pin Configuration

28-Pin DIP, Plastic Miniflat



32-Pin Ceramic Leadless Chip Carrier (LCC)



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Pin Identification

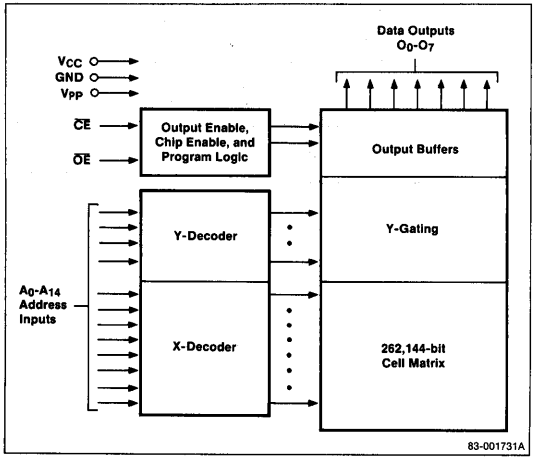
DIP and Plastic Miniflat

No.	Symbol	Function
1	V_{PP}	Program voltage
2-10, 21, 23-27	A_0-A_{14}	Address inputs
11-13, 15-19	O_0-O_7	Data outputs
14	GND	Ground
20	$\overline{CE}$	Chip enable
22	$\overline{OE}$	Output enable
28	V_{CC}	+5 V ±10% power supply

Ceramic LCC

No.	Symbol	Function
1, 12, 17, 26	NC	No connection
2	V_{PP}	Program voltage
3-11, 24, 27-31	A_0-A_{14}	Address inputs
13-15, 18-22	O_0-O_7	Data outputs
16	GND	Ground
23	$\overline{CE}$	Chip enable
25	$\overline{OE}$	Output enable
32	V_{CC}	+5 V ±10% power supply

Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.6 V to +7.0 V
Input voltage, V_{IN}(1)	−0.6 V to V_{CC} + 0.6 V
Output voltage, V_{OUT}	−0.6 V to V_{CC} + 0.6 V
Operating temperature, T_{OPR}	−10°C to 80°C
Storage temperature, T_{STG}	−65°C to 125°C
Program voltage, V_{PP}	−0.6 V to +13.0 V
ID read voltage on pin 24, V_{ID}	−0.6 V to +13.5 V

Note:
(1) V_{IN} = −3.0 V min for 20 ns pulse.

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, f = 1 MHz (Note 1)

		Limits				Test
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	C_{IN}			6	pF	V_{IN} = 0 V
Output capacitance	C_{OUT}			12	pF	V_{OUT} = 0 V

Note:
(1) This parameter is sampled and not 100% tested.

DC Characteristics

Read and Standby Modes

T_A = 0 to +70°C, V_{CC} = +5 V ±10%, V_{PP} = V_{CC}

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC}+0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output leakage current	I_{LO}			10	μA	$\overline{OE}$ = V_{IH}, V_{OUT} = 0 V to V_{CC}
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 V to V_{CC}
Operating supply current	I_{CCA1}			30	mA	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}
Operating supply current	I_{CCA2}			30	mA	5 MHz, I_{OUT} = 0 mA
Standby supply current	I_{SB1}			1	mA	$\overline{CE}$ = V_{IH}
Standby supply current	I_{SB2}			100	μA	$\overline{CE}$ = V_{CC}
Program voltage current	I_{PP1}			100	μA	V_{PP} = V_{CC}

Program, Program Verify, and Program Inhibit Modes

T_A = 25°C ± 5°C, V_{CC} = +6 V ±0.25 V, V_{PP} = +12.5 V ±0.3 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC}+0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
ID read voltage	V_{ID}	11.5		12.5	V	
Input leakage current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Operating supply current	I_{CC}			30	mA	
Program voltage current	I_{PP2}			30	mA	CE = V_{IL}, OE = V_{IH}

AC Characteristics

Read and Standby Modes

T_A = 0 to +70°C, V_{CC} = +5 V ±10%, V_{PP} = V_{CC}

Parameter	Symbol	Limits μPD27C256A-12 Min	Max	μPD27C256A-15(1) Min	Max	μPD27C256A-20(1) Min	Max	Unit	Test Conditions(2)
Address to output delay	t_{ACC}		120		150		200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		120		150		200	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ low to data output delay	t_{OE}		60		75		75	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to data output float delay	t_{DF}		50		60		60	ns	$\overline{CE}$ = V_{IL}
Address to output hold time	t_{OH}	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Notes:

(1) Available in either UV or OTP.

(2) Output load: see figure 1.
Input rise and fall times: 20 ns.
Input pulse levels: 0.45 V to 2.4 V.
Timing measurement reference levels:
Inputs: 0.8 V and 2.0 V
Outputs: 0.8 V and 2.0 V.

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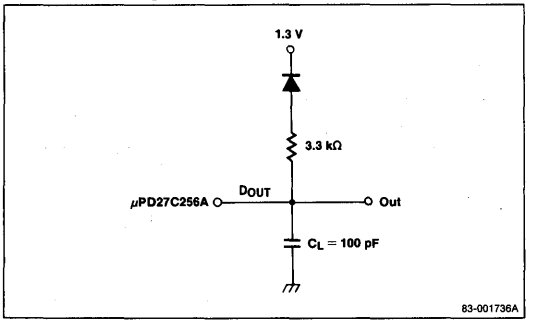
AC Characteristics (cont)

Program, Program Verify, and Program Inhibit Modes
$T_A = 25°C \pm 5°C$, $V_{CC} = +6\ V \pm 0.25\ V$, $V_{PP} = +12.5\ V \pm 0.3\ V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2			μs	(Notes 1, 2, 3)
Data setup time	t_{DS}	2			μs	(Notes 1, 2, 3)
Address hold time	t_{AH}	0			μs	(Notes 1, 2, 3)
Data hold time	t_{DH}	2			μs	(Notes 1, 2, 3)
Output enable to output float delay	t_{DF}			130	ns	(Notes 1, 2, 3)
V_{PP} setup time	t_{VPS}	2			μs	(Notes 1, 2, 3)
Program pulse width	t_{PW}	0.95	1	1.05	ms	(Notes 1, 2, 3)
V_{CC} setup time	t_{VCS}	2			μs	
OE setup time	t_{OES}	2			μs	(Notes 1, 2, 3)
Overprogram pulse width	t_{OPW}	0.95		21	ms	
Data valid from OE	t_{OE}			150	ns	

Notes:
(1) Input pulse levels = 0.45 V to 2.4 V.
(2) Input and output timing reference levels = 0.8 V and 2.0 V.
(3) Input rise and fall times = 20 ns.

Figure 1. Loading Conditions Test Circuit



Truth Table

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A_9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
Program verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	Hi-Z
ID read	V_{IL}	V_{IL}	V_{ID}	V_{CC}	V_{CC}	D_{OUT}

Note:
(1) X can be either V_{IL} or V_{IH}.

Programming Operation

High Speed Programming Mode

Begin programming by erasing all data; this places all bits in the high level (1) state. Enter data by programming a low level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the 8 output pins. Raise V_{CC} to $+6\ V \pm 0.25\ V$; then raise V_{PP} to $+12.5\ V \pm 0.3\ V$. Apply a 1 ms (±5%) program pulse to $\overline{CE}$ as shown in the programming mode timing waveform. The bit is verified and the program/no-program decision is made. If the bit is not programmed, apply another 1 ms pulse to $\overline{CE}$ up to a maximum of 25 times. If the bit is programmed within 25 tries, apply an additional overprogram pulse of (3 × number of tries) ms and input the next address. If the bit is not programmed in 25 tries, reject the device as a program failure.

After all bits are programmed, lower both V_{CC} and V_{PP} to $+5\ V \pm 10\%$ and verify all data again.

Programming Inhibit Mode

Use the programming inhibit mode to program multiple μPD27C256As connected in parallel. All like inputs (except $\overline{CE}$, but including $\overline{OE}$) may be common. Program individual devices by applying a low level (0) TTL pulse to the $\overline{CE}$ input of the μPD27C256A to be programmed. Applying a high level (1) to the $\overline{CE}$ input of the other devices prevents them from being programmed.

Program Verify Mode

Perform verification on the programmed data to determine that the data was correctly programmed. The program verification can be performed with $\overline{OE}$ at a low level (0). To perform verification on multiple μPD27C256As connected in parallel, with a common $\overline{OE}$ input applied to all devices, first reduce V_{PP} to V_{CC}. Then the normal read mode can be used with a low level (0) applied to the $\overline{CE}$ input of the device to be verified. A high level (1) is applied to the $\overline{CE}$ input of all other devices.

Erasure

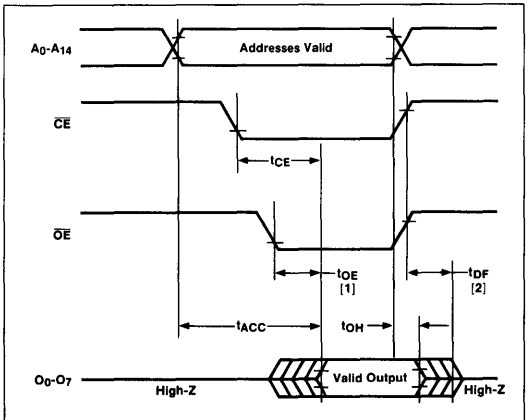
Erase data on the μPD27C256A by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by 254 nm ultraviolet rays. A lighting level of 15 W-sec/cm^2 (min) is required to completely erase written data (ultraviolet ray intensity × exposure time).

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C256A within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

Timing Waveforms

Read Mode



Note:
[1] $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

Program Mode